What is claimed is:

1. A method for forming a volatile memory structure, comprising the steps of:

providing a substrate having a pair of neighboring trenches;

forming a buried trench capacitor in a lower portion of each trench;

forming an asymmetric collar insulating layer, having a high level portion and a low level portion, over an upper portion of the sidewall of each trench, and forming a conductor layer, overlying the buried trench capacitor in each trench, below the surface of the substrate with a lower part of the conductive layer surrounded by the asymmetric collar insulating layer, wherein the high level portion of the asymmetric collar insulating layer is adjacent to the substrate between the neighboring trenches and the low level portion is covered by an upper part of the conductive layer;

forming a dielectric layer overlying the conductive layer in each trench; and

forming two access transistors on the substrate outside of the pair of the neighboring trenches, respectively, wherein the two access transistors have source/drain regions electrically connecting to the conductive layer.

2. The method as claimed in claim 1, wherein the step of forming the asymmetric collar insulating layer and the conductive layer, comprises:

forming a first conductive layer overlying the buried trench capacitor in each trench and surrounded by an insulating spacer protruding the surface of the first conductive layer;

covering portions of the insulating spacers adjacent to the substrate between the neighboring trenches by a masking layer;

removing the uncovered insulating spacers to form the asymmetric collar insulating layer in each trench;

removing the masking layer; and

forming a second conductive layer overlying the first conductive layer, wherein the first conductive layer and the second conductive layer are combined as the conductive layer.

3. The method as claimed in claim 2, wherein the masking layer is a photoresist layer.

4. The method as claimed in claim 1, wherein the step of forming the asymmetric collar insulating layer, comprises:

forming a sacrificial layer overlying the buried trench capacitor in each trench and surrounded by an insulating spacer protruding the surface of the sacrificial layer;

covering portions of the insulating spacers adjacent to the substrate between the neighboring trenches by a masking layer;

removing the uncovered insulating spacers to form the asymmetric collar insulating layer; and

successively removing the masking layer and the sacrificial layer.

5. The method as claimed in claim 4, wherein the sacrificial layer is a photoresist or anti-reflection layer.

6. The method as claimed in claim 4, wherein the masking layer is a photoresist layer.

7. The method as claimed in claim 1, wherein the conductive layer is a doped polysilicon layer.

8. The method as claimed in claim 1, wherein before the step of forming the dielectric layer, further comprises:

forming active area/isolation areas through an active area masking layer.

9. The method as claimed in claim 8, wherein the active area masking layer is a strap type pattern.

10. The method as claimed in claim 1, further forming a gate on the dielectric layer over each trench.

11. A volatile memory structure, comprising:

a substrate having a pair of neighboring trenches;

two buried trench capacitors respectively disposed in a lower portion of the neighboring trenches;

two conductive layers respectively disposed overlying the buried trench capacitor in each trench and below the surface of the substrate;

two asymmetric collar insulating layers respectively disposed over an upper portion of the sidewall of the neighboring trenches and surrounding a lower part of the conductive layers, wherein the asymmetric collar insulating layer has a high level portion and a low level portion, each high level portion is adjacent to the substrate between the neighboring trenches, and each low level portion is covered by an upper part of the conductive layer;

two dielectric layers respectively disposed overlying the conductive layer in each trench; and

two access transistors respectively disposed overlying the substrate outside of the pair of the neighboring trenches and having source/drain regions electrically connecting to the conductive layers, respectively.

12. The volatile memory structure as claimed in claim 11, further comprising two gates respectively disposed overlying the dielectric layer over each trench.

13. The volatile memory structure as claimed in claim 11, wherein the conductive layer is a doped polysilicon layer.

14. A method for forming a trench capacitor structure for a volatile memory device, comprising the steps of:

providing a substrate having a trench;

forming a buried bottom plate in the substrate around a lower portion of the trench;

forming a capacitor dielectric layer over a lower portion of the sidewall of the trench ;

forming a top plate in the trench and surrounded by the capacitor dielectric layer;

forming an asymmetric collar oxide layer, having a high level portion and a low level portion, over an upper portion of the sidewall of the trench, and forming a conductive layer, overlying the top plate in the trench, below the surface of the substrate with a lower part of the conductive layer surrounded by the asymmetric collar oxide layer, wherein the low level portion of the asymmetric collar oxide layer is covered by an upper part of the conductive layer; and

forming a dielectric layer overlying the conductive layer in the trench.

15. The method as claimed in claim 14, wherein the step of forming the asymmetric collar oxide layer and the conductive layer, comprises:

forming a first conductive layer overlying the top plate in the trench and surrounded by an oxide spacer protruding the surface of the first conductive layer;

covering a portion of the oxide spacer by a masking layer;

removing the uncovered oxide spacer to form the asymmetric collar oxide layer in the trench;

removing the masking layer; and

forming a second conductive layer overlying the first conductive layer, wherein the first conductive layer and the second conductive layer are combined as the conductive layer.

16. The method as claimed in claim 15, wherein the masking layer is a photoresist layer.

17. The method as claimed in claim 14, wherein the step of forming the asymmetric collar oxide layer, comprises:

forming a sacrificial layer overlying the top plate in the trench and surrounded by an oxide spacer protruding the surface of the first masking layer;

covering a portion of the oxide spacer by a masking layer;

removing the uncovered oxide spacer to form the asymmetric collar oxide layer; and

successively removing the masking layer and the sacrificial layer.

18. The method as claimed in claim 17, wherein the sacrificial layer is a photoresist or anti-reflection layer.

19. The method as claimed in claim 17, wherein the masking layer is a photoresist layer.

20. The method as claimed in claim 14, wherein the conductive layer is a doped polysilicon layer.

21. The method as claimed in claim 14, wherein before the step of forming the dielectric layer, further comprises:
forming active area/isolation areas through an active area masking layer.

22. The method as claimed in claim 21, wherein the active area masking layer is a strap type pattern.

23. A trench capacitor structure for a volatile memory device, comprising:
a substrate having a trench;
a buried bottom plate formed in the substrate around a lower portion of the trench;
a capacitor dielectric layer disposed in the lower portion of the trench;
a top plate disposed in the trench and surrounded by the capacitor dielectric layer;
a conductive layer disposed overlying the top plate in the trench and below the surface of the substrate;
an asymmetric collar oxide layer disposed over an upper portion of the sidewall of the trench and surrounding a lower part of the conductive layer, wherein the asymmetric collar oxide layer has a low level portion covered by an upper part of the conductive layer; and

a dielectric layer disposed overlying the conductive layer in the trench.

24. The trench capacitor structure as claimed in claim 23, wherein the conductive layer is a doped polysilicon layer.